Phase-locked loop

A **phase-locked loop** or **phase lock loop** (**PLL**) is a control system that generates an output signal whose phase is fixed relative to the phase of an input signal. Keeping the input and output phase in lockstep also implies keeping the input and output frequencies the same, thus a phase-locked loop can also track an input frequency. And by incorporating a frequency divider, a PLL can generate a stable frequency that is a multiple of the input frequency.

These properties are used for clock synchronization, demodulation, frequency synthesis, clock multipliers, and signal recovery from a noisy communication channel. Since 1969, a single integrated circuit can provide a complete PLL building block, and nowadays have output frequencies from a fraction of a hertz up to many gigahertz. Thus, PLLs are widely employed in radio, telecommunications, computers (e.g. to distribute precisely timed clock signals in microprocessors), grid-tie inverters (electronic power converters used to integrate DC renewable resources and storage elements such as photovoltaics and batteries with the power grid), and other electronic applications.

Simple example

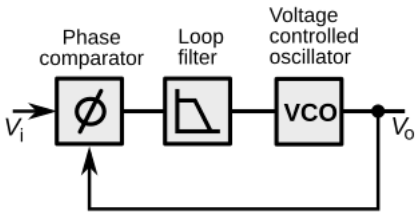


Figure 1. Simple analog phase locked loop

A simple analog PLL is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop (Figure 1). The oscillator generates a periodic signal V_o with frequency proportional to an applied voltage, hence the term voltage-controlled oscillator (VCO). The phase detector compares the phase of the VCO's output signal with the phase of periodic input reference signal V_i and outputs a voltage (stabilized by the filter) to adjust the oscillator's frequency to match the phase of V_o to the phase of V_i.

Clock analogy

Phase can be proportional to time,[a] so a phase difference can correspond to a time difference.

Left alone, different clocks will mark time at slightly different rates. A mechanical clock, for example, might be fast or slow by a few seconds per hour compared to a reference atomic clock (such as the NIST-F2). That time difference becomes substantial over time. Instead, the owner can synchronize their mechanical clock (with varying degrees of accuracy) by phase-locking it to a reference clock.

An inefficient synchronization method involves the owner resetting their clock to that more accurate clock's time every week. But, left alone, their clock will still continue to diverge from the reference clock at the same few seconds per hour rate.

A more efficient synchronization method (analogous to the simple PLL in Figure 1) utilizes the fast-slow timing adjust control (analogous to how the VCO's frequency can be adjusted) available on some clocks. Analogously to the phase comparator, the owner could notice their clock's misalignment and turn its timing adjust a small proportional amount to make their clock's frequency a little slower (if their clock was fast) or faster (if their clock was slow). If they don't overcompensate, then their clock will be more accurate than before. Over a series of such weekly adjustments, their clock's notion of a second would agree close enough with the reference clock, so they could be said to be locked both in frequency and phase.

An early electromechanical version of a phase-locked loop was used in 1921 in the Shortt-Synchronome clock.

History

Spontaneous synchronization of weakly coupled pendulum clocks was noted by the Dutch physicist Christiaan Huygens as early as 1673.[1] Around the turn of the 19th century, Lord Rayleigh observed synchronization of weakly coupled organ pipes and tuning forks.[2] In 1919, W. H. Eccles and J. H. Vincent found that two electronic oscillators that had been tuned to oscillate at slightly different frequencies but that were coupled to a resonant circuit would soon oscillate at the same frequency.[3] Automatic synchronization of electronic oscillators was described in 1923 by Edward Victor Appleton.[4]

In 1925, David Robertson, first professor of electrical engineering at the University of Bristol, introduced phase locking in his clock design to control the striking of the bell Great George in the new Wills Memorial Building. Robertson's clock incorporated an electromechanical device that could vary the rate of oscillation of the pendulum, and derived correction signals from a circuit that compared the pendulum phase with that of an incoming telegraph pulse from Greenwich Observatory every morning at 10:00 GMT. Including equivalents of every element of a modern

electronic PLL, Robertson's system was notably ahead of its time in that its phase detector was a relay logic implementation of the transistor circuits for phase/frequency detectors not seen until the 1970s.

Robertson's work predated research towards what was later named the phase-lock loop in 1932, when British researchers developed an alternative to Edwin Armstrong's superheterodyne receiver, the Homodyne or direct-conversion receiver. In the homodyne or synchrodyne system, a local oscillator was tuned to the desired input frequency and multiplied with the input signal. The resulting output signal included the original modulation information. The intent was to develop an alternative receiver circuit that required fewer tuned circuits than the superheterodyne receiver. Since the local oscillator would rapidly drift in frequency, an automatic correction signal was applied to the oscillator, maintaining it in the same phase and frequency of the desired signal. The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal *L'Onde Électrique*.[5][6][7]

In analog television receivers since at least the late 1930s, phase-locked-loop horizontal and vertical sweep circuits are locked to synchronization pulses in the broadcast signal.[8]

ON Semiconductor HC4046A

In 1969, Signetics introduced a line of low-cost monolithic integrated circuits like the NE565 using bipolar transistors, that were complete phase-locked loop systems on a chip,[9] and applications for the technique multiplied. A few years later, RCA introduced the CD4046 Micropower Phase-Locked Loop using CMOS, which also became a popular integrated circuit building block.

Structure and function

Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure.

Analog PLL circuits include four basic elements:

- Phase detector
- Low-pass filter

- Voltage controlled oscillator
- Feedback path, which may include a frequency divider

Variations

There are several variations of PLLs. Some terms that are used are "analog phase-locked loop" (APLL), also referred to as a linear phase-locked loop" (LPLL), "digital phase-locked loop" (DPLL), "all digital phase-locked loop" (ADPLL), and "software phase-locked loop" (SPLL).[10]

Analog or linear PLL (APLL)
: Phase detector is an analog multiplier. Loop filter is active or passive. Uses a voltage-controlled oscillator (VCO). APLL is said to be a *type II* if its loop filter has transfer function with exactly one pole at the origin (see also Egan's conjecture on the pull-in range of type II APLL).

Digital PLL (DPLL)
: An analog PLL with a digital phase detector (such as XOR, edge-triggered JK flip flop, phase frequency detector). May have digital divider in the loop.

All digital PLL (ADPLL)
: Phase detector, filter and oscillator are digital. Uses a numerically controlled oscillator (NCO).

Neuronal PLL (NPLL)
: Phase detector is implemented by neuronal non-linearity, oscillator by rate-controlled oscillating neurons.[11]

Software PLL (SPLL)
: Functional blocks are implemented by software rather than specialized hardware.

Charge-pump PLL (CP-PLL)
: CP-PLL is a modification of phase-locked loops with phase-frequency detector and square waveform signals. See also Gardner's conjecture on CP-PLL.

Performance parameters

- Type and order.
- Frequency ranges: hold-in range (tracking range), pull-in range (capture range, acquisition range), lock-in range.[12] See also Gardner's problem on the lock-in range, Egan's conjecture on the pull-in range of type II APLL, Viterbi's problem on the PLL ranges coincidence.
- Loop bandwidth: Defining the speed of the control loop.
- Transient response: Like overshoot and settling time to a certain accuracy (like 50 ppm).
- Steady-state errors: Like remaining phase or timing error.
- Output spectrum purity: Like sidebands generated from a certain VCO tuning voltage ripple.

- Phase-noise: Defined by noise energy in a certain frequency band (like 10 kHz offset from carrier). Highly dependent on VCO phase-noise, PLL bandwidth, etc.
- General parameters: Such as power consumption, supply voltage range, output amplitude, etc.

Applications

Phase-locked loops are widely used for synchronization purposes; in space communications for coherent demodulation and threshold extension, bit synchronization, and symbol synchronization. Phase-locked loops can also be used to demodulate frequency-modulated signals. In radio transmitters, a PLL is used to synthesize new frequencies which are a multiple of a reference frequency, with the same stability as the reference frequency.[13]

Other applications include:

- Demodulation of frequency modulation (FM): If PLL is locked to an FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated out. Since the VCO used in an integrated-circuit PLL is highly linear, it is possible to realize highly linear FM demodulators.
- Demodulation of frequency-shift keying (FSK): In digital data communication and computer peripherals, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies.
- Recovery of small signals that otherwise would be lost in noise (lock-in amplifier to track the reference frequency)
- Recovery of clock timing information from a data stream such as from a disk drive
- Clock multipliers in microprocessors that allow internal processor elements to run faster than external connections, while maintaining precise timing relationships
- Demodulation of modems and other tone signals for telecommunications and remote control.
- DSP of video signals; Phase-locked loops are also used to synchronize phase and frequency to the input analog video signal so it can be sampled and digitally processed
- Atomic force microscopy in frequency modulation mode, to detect changes of the cantilever resonance frequency due to tip–surface interactions
- DC motor drive

Clock recovery

Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then uses a PLL to phase-align it to the data stream's signal edges. This process is referred to as clock recovery. For this scheme to work, the data stream must have edges frequently-enough to correct any drift in the PLL's oscillator. Thus a line code with a hard upper bound on the maximum time between edges (e.g. 8b/10b encoding) is typically used to encode the data.

Deskewing

If a clock is sent in parallel with data, that clock can be used to sample the data. Because the clock must be received and amplified before it can drive the flip-flops which sample the data, there will be a finite, and process-, temperature-, and voltage-dependent delay between the detected clock edge and the received data window. This delay limits the frequency at which data can be sent. One way of eliminating this delay is to include a deskew PLL on the receive side, so that the clock at each data flip-flop is phase-matched to the received clock. In that type of application, a special form of a PLL called a delay-locked loop (DLL) is frequently used.[14]

Clock generation

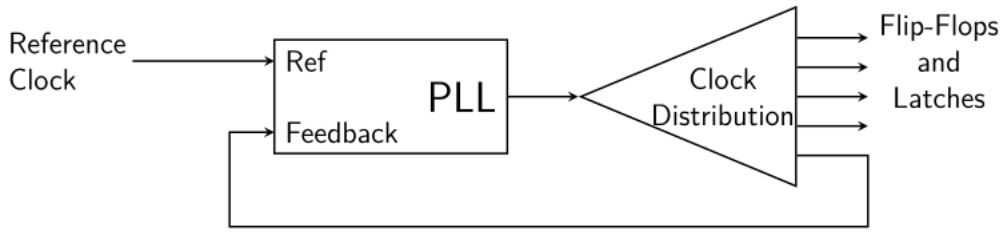
Many electronic systems include processors of various sorts that operate at hundreds of megahertz to gigahertz, well above the practical frequencies of crystal oscillators. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertz and the reference crystal is just tens or hundreds of megahertz.

Spread spectrum

All electronic systems emit some unwanted radio frequency energy. Various regulatory agencies (such as the FCC in the United States) put limits on the emitted energy and any interference caused by it. The emitted noise generally appears at sharp spectral peaks (usually at the operating frequency of the device, and a few harmonics). A system designer can use a spread-spectrum PLL

to reduce interference with high-Q receivers by spreading the energy over a larger portion of the spectrum. For example, by changing the operating frequency up and down by a small amount (about 1%), a device running at hundreds of megahertz can spread its interference evenly over a few megahertz of spectrum, which drastically reduces the amount of noise seen on broadcast FM radio channels, which have a bandwidth of several tens of kilohertz.

Clock distribution



Typically, the reference clock enters the chip and drives a phase locked loop (PLL), which then drives the system's clock distribution. The clock distribution is usually balanced so that the clock arrives at every endpoint simultaneously. One of those endpoints is the PLL's feedback input. The function of the PLL is to compare the distributed clock to the incoming reference clock, and vary the phase and frequency of its output until the reference and feedback clocks are phase and frequency matched.

PLLs are ubiquitous—they tune clocks in systems several feet across, as well as clocks in small portions of individual chips. Sometimes the reference clock may not actually be a pure clock at all, but rather a data stream with enough transitions that the PLL is able to recover a regular clock from that stream. Sometimes the reference clock is the same frequency as the clock driven through the clock distribution, other times the distributed clock may be some rational multiple of the reference.

AM detection

A PLL may be used to synchronously demodulate amplitude modulated (AM) signals. The PLL recovers the phase and frequency of the incoming AM signal's carrier. The recovered phase at the VCO differs from the carrier's by 90°, so it is shifted in phase to match, and then fed to a multiplier. The output of the multiplier contains both the sum and the difference frequency signals, and the demodulated output is obtained by low-pass filtering. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak type AM demodulators. However, the loop may lose lock where AM signals have 100% modulation depth.[15]

Jitter and noise reduction

One desirable property of all PLLs is that the reference and feedback clock edges be brought into very close alignment. The average difference in time between the phases of the two signals when the PLL has achieved lock is called the **static phase offset** (also called the **steady-state phase error**). The variance between these phases is called **tracking jitter**. Ideally, the static phase offset should be zero, and the tracking jitter should be as low as possible.

Phase noise is another type of jitter observed in PLLs, and is caused by the oscillator itself and by elements used in the oscillator's frequency control circuit. Some technologies are known to perform better than others in this regard. The best digital PLLs are constructed with emitter-coupled logic (ECL) elements, at the expense of high power consumption. To keep phase noise low in PLL circuits, it is best to avoid saturating logic families such as transistor-transistor logic (TTL) or CMOS.[16]

Another desirable property of all PLLs is that the phase and frequency of the generated clock be unaffected by rapid changes in the voltages of the power and ground supply lines, as well as the voltage of the substrate on which the PLL circuits are fabricated. This is called substrate and supply noise rejection. The higher the noise rejection, the better.

To further improve the phase noise of the output, an injection locked oscillator can be employed following the VCO in the PLL.

Frequency synthesis

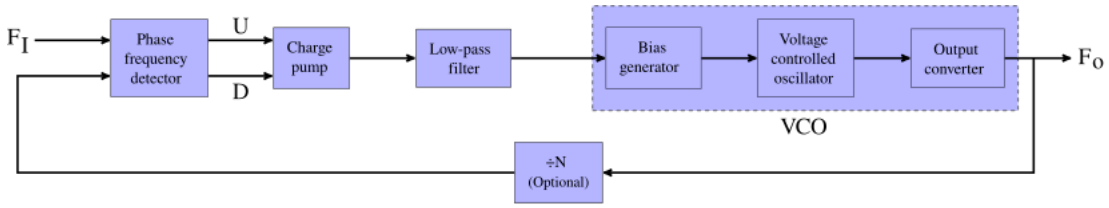
In digital wireless communication systems (GSM, CDMA etc.), PLLs are used to provide the local oscillator up-conversion during transmission and down-conversion during reception. In most cellular handsets this function has been largely integrated into a single integrated circuit to reduce the cost and size of the handset. However, due to the high performance required of base station terminals, the transmission and reception circuits are built with discrete components to achieve the levels of performance required. GSM local oscillator modules are typically built with a frequency synthesizer integrated circuit and discrete resonator VCOs.

Phase angle reference

Grid-tie inverters based on voltage source inverters source or sink real power into the AC electric grid as a function of the phase angle of the voltage they generate relative to the grid's voltage phase angle, which is measured using a PLL. In photovoltaic applications, the more the sine wave

produced leads the grid voltage wave, the more power is injected into the grid. For battery applications, the more the sine wave produced lags the grid voltage wave, the more the battery charges from the grid, and the more the sine wave produced leads the grid voltage wave, the more the battery discharges into the grid.

Block diagram



Block diagram of a phase-locked loop

The block diagram shown in the figure shows an input signal, F_I, which is used to generate an output, F_O. The input signal is often called the *reference signal* (also abbreviated F_{REF}).[17]

At the input, a phase detector (shown as the Phase frequency detector and Charge pump blocks in the figure) compares two input signals, producing an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a VCO which creates an output phase. The output is fed through an optional divider back to the input of the system, producing a negative feedback loop. If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase of the input.

Analog phase locked loops are generally built with an analog phase detector, low-pass filter and VCO placed in a negative feedback configuration. A digital phase locked loop uses a digital phase detector; it may also have a divider in the feedback path or in the reference path, or both, in order to make the PLL's output signal frequency a rational multiple of the reference frequency. A non-integer multiple of the reference frequency can also be created by replacing the simple divide-by-*N* counter in the feedback path with a programmable pulse swallowing counter. This technique is usually referred to as a fractional-N synthesizer or fractional-N PLL.

The oscillator generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. If the phase from the oscillator falls behind that of the reference, the phase detector changes the control voltage of the oscillator so that it speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs. Depending on the application, either the output of the

controlled oscillator, or the control signal to the oscillator, provides the useful output of the PLL system.

Elements

Phase detector

A phase detector (PD) generates a voltage, which represents the phase difference between two signals. In a PLL, the two inputs of the phase detector are the reference input and the feedback from the VCO. The PD output voltage is used to control the VCO such that the phase difference between the two inputs is held constant, making it a negative feedback system. [18]

Different types of phase detectors have different performance characteristics.

For instance, the frequency mixer produces harmonics that adds complexity in applications where spectral purity of the VCO signal is important. The resulting unwanted (spurious) sidebands, also called "reference spurs" can dominate the filter requirements and reduce the capture range well below or increase the lock time beyond the requirements. In these applications the more complex digital phase detectors are used which do not have as severe a reference spur component on their output. Also, when in lock, the steady-state phase difference at the inputs using this type of phase detector is near 90 degrees.

In PLL applications it is frequently required to know when the loop is out of lock. The more complex digital phase-frequency detectors usually have an output that allows a reliable indication of an out of lock condition.

An XOR gate is often used for digital PLLs as an effective yet simple phase detector. It can also be used in an analog sense with only slight modification to the circuitry.

Filter

The block commonly called the PLL loop filter (usually a low-pass filter) generally has two distinct functions.

The primary function is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at startup. Common considerations are the range over which the loop can achieve lock (pull-in range, lock range or capture range), how fast the loop achieves lock (lock time, lock-up time

or settling time) and damping behavior. Depending on the application, this may require one or more of the following: a simple proportion (gain or attenuation), an integral (low-pass filter) and/or derivative (high-pass filter). Loop parameters commonly examined for this are the loop's gain margin and phase margin. Common concepts in control theory including the PID controller are used to design this function.

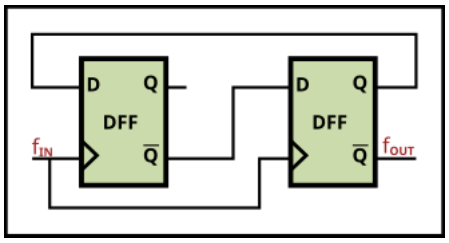
The second common consideration is limiting the amount of reference frequency energy (ripple) appearing at the phase detector output that is then applied to the VCO control input. This frequency modulates the VCO and produces FM sidebands commonly called "reference spurs".

The design of this block can be dominated by either of these considerations, or can be a complex process juggling the interactions of the two. The typical trade-off of increasing the bandwidth is degraded stability. Conversely, the tradeoff of extra damping for better stability is reduced speed and increased settling time. Often the phase-noise is also affected.[13]

Oscillator

All phase-locked loops employ an oscillator element with variable frequency capability. This can be an analog VCO either driven by analog circuitry in the case of an APLL or driven digitally through the use of a digital-to-analog converter as is the case for some DPLL designs. Pure digital oscillators such as a numerically controlled oscillator are used in ADPLLs.

Feedback path and optional divider



An example digital divider (by 4) for use in the feedback path of a multiplying PLL

PLLs may include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio transmitter applications and for computer clocking, since a large number of frequencies can be produced from a single stable, accurate, quartz crystal–controlled reference oscillator (which were expensive before commercial-scale hydrothermal synthesis provided cheap synthetic quartz).

Some PLLs also include a divider between the reference clock and the reference input to the phase detector. If the divider in the feedback path divides by N and the reference input divider divides by M, it allows the PLL to multiply the reference frequency by N/M. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful.

Frequency multiplication can also be attained by locking the VCO output to the *N*th harmonic of the reference signal. Instead of a simple phase detector, the design uses a harmonic mixer (sampling mixer). The harmonic mixer turns the reference signal into an impulse train that is rich in harmonics.[b] The VCO output is coarse tuned to be close to one of those harmonics. Consequently, the desired harmonic mixer output (representing the difference between the *N* harmonic and the VCO output) falls within the loop filter passband.

It should also be noted that the feedback is not limited to a frequency divider. This element can be other elements such as a frequency multiplier, or a mixer. The multiplier will make the VCO output a sub-multiple (rather than a multiple) of the reference frequency. A mixer can translate the VCO frequency by a fixed offset. It may also be a combination of these. For example, a divider following a mixer allows the divider to operate at a much lower frequency than the VCO without a loss in loop gain.

Modeling

Time domain model of APLL

The equations governing a phase-locked loop with an analog multiplier as the phase detector and linear filter may be derived as follows. Let the input to the phase detector be $f_1(\theta_1(t))$ and the output of the VCO is $f_2(\theta_2(t))$ with phases $\theta_1(t)$ and $\theta_2(t)$. The functions $f_1(\theta)$ and $f_2(\theta)$ describe waveforms of signals. Then the output of the phase detector $\varphi(t)$ is given by

$$\varphi(t) = f_1(\theta_1(t)) f_2(\theta_2(t))$$

The VCO frequency is usually taken as a function of the VCO input $g(t)$ as

$$\dot{\theta}_2(t) = \omega_2(t) = \omega_{\text{free}} + g_v g(t)$$

where g_v is the *sensitivity* of the VCO and is expressed in Hz / V; ω_{free} is a free-running frequency of VCO.

The loop filter can be described by a system of linear differential equations

$$\begin{aligned} \dot{x} &= Ax + b\varphi(t), \\ g(t) &= c^* x, \end{aligned} \qquad x(0) = x_0,$$

where $\varphi(t)$ is an input of the filter, $g(t)$ is an output of the filter, A is n-by-n matrix, $x \in \mathbb{C}^n, \quad b \in \mathbb{R}^n, \quad c \in \mathbb{C}^n, \quad . x_0 \in \mathbb{C}^n$ represents an initial state of the filter. The star symbol is a conjugate transpose.

Hence the following system describes PLL

$$\begin{aligned} \dot{x} &= Ax + bf_1(\theta_1(t))f_2(\theta_2(t)), \\ \dot{\theta}_2 &= \omega_{\text{free}} + g_v(c^* x) \end{aligned} \qquad x(0) = x_0, \quad \theta_2(0) = \theta_0.$$

where θ_0 is an initial phase shift.

Phase domain model of APLL

Consider the input of PLL $f_1(\theta_1(t))$ and VCO output $f_2(\theta_2(t))$ are high frequency signals. Then for any piecewise differentiable 2π-periodic functions $f_1(\theta)$ and $f_2(\theta)$ there is a function $\varphi(\theta)$ such that the output $G(t)$ of Filter

$$\begin{aligned} \dot{x} &= Ax + b\varphi(\theta_1(t) - \theta_2(t)), \\ G(t) &= c^* x, \end{aligned} \qquad x(0) = x_0,$$

in phase domain is asymptotically equal (the difference $G(t) - g(t)$ is small with respect to the frequencies) to the output of the Filter in time domain model. [19] [20] Here function $\varphi(\theta)$ is a phase detector characteristic.

Denote by $\theta_\Delta(t)$ the phase difference

$$\theta_\Delta = \theta_1(t) - \theta_2(t).$$

Then the following dynamical system describes PLL behavior

$$\begin{aligned} \dot{x} &= Ax + b\varphi(\theta_\Delta), \\ \dot{\theta}_\Delta &= \omega_\Delta - g_v(c^* x). \end{aligned} \qquad x(0) = x_0, \quad \theta_\Delta(0) = \theta_1(0) - \theta_2(0).$$

Here $\omega_\Delta = \omega_1 - \omega_{\text{free}}$; ω_1 is the frequency of a reference oscillator (we assume that ω_{free} is constant).

Example

Consider sinusoidal signals

$$f_1(\theta_1(t)) = A_1 \sin(\theta_1(t)), \quad f_2(\theta_2(t)) = A_2 \cos(\theta_2(t))$$

and a simple one-pole RC circuit as a filter. The time-domain model takes the form

$$\dot{x} = -\frac{1}{RC}x + \frac{1}{RC}A_1 A_2 \sin(\theta_1(t))\cos(\theta_2(t)),$$

$$\dot{\theta}_2 = \omega_{\text{free}} + g_v(c^* x)$$

PD characteristics for this signals is equal[21] to

$$\varphi(\theta_1 - \theta_2) = \frac{A_1 A_2}{2}\sin(\theta_1 - \theta_2)$$

Hence the phase domain model takes the form

$$\dot{x} = -\frac{1}{RC}x + \frac{1}{RC}\frac{A_1 A_2}{2}\sin(\theta_\Delta),$$

$$\dot{\theta}_\Delta = \omega_\Delta - g_v(c^* x).$$

This system of equations is equivalent to the equation of mathematical pendulum

$$x = \frac{\dot{\theta}_2 - \omega_2}{g_v c^*} = \frac{\omega_1 - \dot{\theta}_\Delta - \omega_2}{g_v c^*},$$

$$\dot{x} = \frac{\ddot{\theta}_2}{g_v c^*},$$

$$\theta_1 = \omega_1 t + \Psi,$$

$$\theta_\Delta = \theta_1 - \theta_2,$$

$$\dot{\theta}_\Delta = \dot{\theta}_1 - \dot{\theta}_2 = \omega_1 - \dot{\theta}_2,$$

$$\frac{1}{g_v c^*}\ddot{\theta}_\Delta - \frac{1}{g_v c^* RC}\dot{\theta}_\Delta - \frac{A_1 A_2}{2RC}\sin\theta_\Delta = \frac{\omega_2 - \omega_1}{g_v c^* RC}.$$

Linearized phase domain model

Phase locked loops can also be analyzed as control systems by applying the Laplace transform. The loop response can be written as

$$\frac{\theta_o}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)}$$

Where

- θ_o is the output phase in radians
- θ_i is the input phase in radians

- K_p is the phase detector gain in volts per radian
- K_v is the VCO gain in radians per volt-second
- $F(s)$ is the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. The loop transfer function in this case is

$$F(s) = \frac{1}{1 + sRC}$$

The loop response becomes:

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

This is the form of a classic harmonic oscillator. The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

where ζ is the damping factor and ω_n is the natural frequency of the loop.

For the one-pole RC filter,

$$\omega_n = \sqrt{\frac{K_p K_v}{RC}}$$
$$\zeta = \frac{1}{2\sqrt{K_p K_v RC}}$$

The loop natural frequency is a measure of the response time of the loop, and the damping factor is a measure of the overshoot and ringing. Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping). With a single pole filter, it is not possible to control the loop frequency and damping factor independently. For the case of critical damping,

$$RC = \frac{1}{2K_p K_v}$$
$$\omega_c = K_p K_v \sqrt{2}$$

A slightly more effective filter, the lag-lead filter includes one pole and one zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

This filter has two time constants

$$\tau_1 = C(R_1 + R_2)$$
$$\tau_2 = CR_2$$

Substituting above yields the following natural frequency and damping factor

$$\omega_n = \sqrt{\frac{K_p K_v}{\tau_1}}$$
$$\zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$
$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

Real world loop filter design can be much more complex e.g. using higher order filters to reduce various types or source of phase noise. (See the D Banerjee ref below)

Implementing a digital phase-locked loop in software

Digital phase locked loops can be implemented in hardware, using integrated circuits such as a CMOS 4046. However, with microcontrollers becoming faster, it may make sense to implement a phase locked loop in software for applications that do not require locking onto signals in the MHz range or faster, such as precisely controlling motor speeds. Software implementation has several advantages including easy customization of the feedback loop including changing the multiplication or division ratio between the signal being tracked and the output oscillator. Furthermore, a software implementation is useful to understand and experiment with. As an example of a phase-locked loop implemented using a phase frequency detector is presented in MATLAB, as this type of phase detector is robust and easy to implement.

```
% This example is written in MATLAB

% Initialize variables
vcofreq = zeros(1, numiterations);
ervec = zeros(1, numiterations);
% Keep track of last states of reference, signal, and error signal
```

```
qsig = 0; qref = 0; lref = 0; lsig = 0; lersig = 0;
phs = 0;
freq = 0;

% Loop filter constants (proportional and derivative)
% Currently powers of two to facilitate multiplication by shifts
prop = 1 / 128;
deriv = 64;

for it = 1:numiterations
    % Simulate a local oscillator using a 16-bit counter
    phs = mod(phs + floor(freq / 2 ^ 16), 2 ^ 16);
    ref = phs < 32768;
    % Get the next digital value (0 or 1) of the signal to track
    sig = tracksig(it);
    % Implement the phase-frequency detector
    rst = ~ (qsig & qref); % Reset the "flip-flop" of the phase-
frequency
    % detector when both signal and reference are high
    qsig = (qsig | (sig & ~ lsig)) & rst; % Trigger signal flip-flop
and leading edge of signal
    qref = (qref | (ref & ~ lref)) & rst; % Trigger reference flip-
flop on leading edge of reference
    lref = ref; lsig = sig; % Store these values for next iteration
(for edge detection)
    ersig = qref - qsig; % Compute the error signal (whether
frequency should increase or decrease)
    % Error signal is given by one or the other flip flop signal
    % Implement a pole-zero filter by proportional and derivative
input to frequency
    filtered_ersig = ersig + (ersig - lersig) * deriv;
    % Keep error signal for proportional output
    lersig = ersig;
    % Integrate VCO frequency using the error signal
    freq = freq - 2 ^ 16 * filtered_ersig * prop;
    % Frequency is tracked as a fixed-point binary fraction
    % Store the current VCO frequency
    vcofreq(1, it) = freq / 2 ^ 16;
    % Store the error signal to show whether signal or reference is
higher frequency
    ervec(1, it) = ersig;
end
```

In this example, an array `tracksig` is assumed to contain a reference signal to be tracked. The oscillator is implemented by a counter, with the most significant bit of the counter indicating the on/off status of the oscillator. This code simulates the two D-type flip-flops that comprise a phase-frequency comparator. When either the reference or signal has a positive edge, the

corresponding flip-flop switches high. Once both reference and signal is high, both flip-flops are reset. Which flip-flop is high determines at that instant whether the reference or signal leads the other. The error signal is the difference between these two flip-flop values. The pole-zero filter is implemented by adding the error signal and its derivative to the filtered error signal. This in turn is integrated to find the oscillator frequency.

In practice, one would likely insert other operations into the feedback of this phase-locked loop. For example, if the phase locked loop were to implement a frequency multiplier, the oscillator signal could be divided in frequency before it is compared to the reference signal.

See also

- Frequency-locked loop
- Charge-pump phase-locked loop
- Carrier recovery
- Circle map – A simple mathematical model of the phase-locked loop showing both mode-locking and chaotic behavior.
- Costas loop
- Delay-locked loop (DLL)
- Direct conversion receiver
- Direct digital synthesizer
- Kalman filter
- PLL multibit
- Shortt–Synchronome clock – Slave pendulum phase-locked to master (ca 1921)

Notes

a. If the frequency is constant and the initial phase is zero, then the phase of a sinusoid is proportional to time.

b. Typically, the reference sinewave drives a step recovery diode circuit to make this impulse train. The resulting impulse train drives a sample gate.

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   - Lord Rayleigh, *The Theory of Sound* (London, England: Macmillan, 1896), vol. 2. The synchronization of organ pipes in opposed phase is mentioned in §322c, pages 221–222. (https://archive.org/details/theorysound05raylgoog/page/n239)
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3. See:
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6. See also: French patent no. 635,451 (filed: 6 October 1931; issued: 29 September 1932); and U.S. patent "Synchronizing system" (http://patimg1.uspto.gov/.piw?Docid=01990428&homeurl=http%3A%2F%2Fpatft.uspto.gov%2Fnetacgi%2Fnph-Parser%3FSect1%3DPTO2%2526Sect2%3DHITOFF%2526p%3D1%2526u%3D%25252Fnetahtml%25252FPTO%25252Fsearch-bool.html%2526r%3D1%2526f%3DG%2526l%3D50%2526co1%3DAND%2526d%3DPALL%2526s1%3D1,990,428.PN.%2526OS%3DPN%2F1,990,428%2526RS%3DPN%2F1,990,428&PageNum=&Rtype=&SectionNum=&idkey=NONE&Input=View+first+page) , no. 1,990,428 (filed: 29 September 1932; issued: 5 February 1935).
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External links

- Phase locked loop primer (https://www.electronics-notes.com/articles/radio/pll-phase-locked-loop/tutorial-primer-basics.php) – Includes embedded video

- Excel Unusual hosts an animated PLL model (http://www.excelunusual.com/preview-2/) and the tutorials to code such a model (http://www.excelunusual.com/a-phase-locked-loop-pll-model-video-preview/) .